Bit Error Rate FPGA Specification



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Revision History

|  |  |  |
| --- | --- | --- |
| Date | Version | Description |
| 3/26/2014 | 1.0 | First publish |
| 10/17/2023 | 2.0 | Major changes to BER and internal data collection |
| 12/8/2023 | 2.1 | Updated the description for modules and registers |
|  |  |  |

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# Introduction

## Overview

This FPGA design is used during manufacturing of the TVS to fully test the functionality of the TVS assembly, including daughter board interfaces, LVDS, RS422, and LVTTL transceivers, and front panel connectors. This FPGA design optimizes the test process by allowing the user to connect and disconnect loopback plugs without any intermediate user input. The FPGA keeps track of successful loopback connectivity for each input and each output. Using a pseudo-random bit stream, the FPGA design is able to verify signal integrity using bit error rate testing of each signal at the following frequencies.

|  |  |
| --- | --- |
| Type | Frequency |
| LVTTL | 1MHz |
| RS422 | 30MHz |
| LVDS | 150MHz |

## Applicable Documents

The following documents contain background material that may be referenced in this document.

|  |  |  |
| --- | --- | --- |
| Document Number | Date | Title |
| ING-TVS-SPEC-001 | - | TVS User’s Manual |
|  |  |  |
|  |  |  |

# Block Diagram

A computer screen shot of a computer program

Description automatically generated

Figure 1 FPGA Block Diagram

# Hardware Description

## Signal Generator

This block generates a pseudo-random bit stream that is 223 bits long repeatedly. The PN23 is ideal for making eye pattern measurements. The PN23 uses a Fibonacci-style LFSR with the equation:

Additionally, to improve test speed and responsiveness, this block generates pulses for each connector on the TVS until activity is detected on a receiving end.

## Sync

When a signal is detected on one of the mux addresses that signal is then forwarded to the BER counter along with the address of the received signal. Additionally, a signal to hold the mux and Demux addresses for testing is issued to the Signal Control block.

## Mux

The mux block connects one of the TVS inputs to the Sync Check block. During the test any received signal will be recaptured by the Mux block via combinatorial logic. Once a signal is selected it is sampled by both edges of the input clock allowing for proper signal capturing despite unknown delays along the TVS loop backs.

## Demux

The demux block connects the single PN23 output to each of the TVS outputs. The Demux select signals are driven by the Signal Control block, rotating through each valid input and output pair.

The demux/mux blocks operate in two steps as shown in the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| Mux Address | Name | Demux Address | Name |
| 0x027 – 0x000 | RS422In[0:39] | **0x00F – 0x000** | RS422Out[0:15] |
| 0x02B – 0x028 | UartIn[0:3] | **0x013 – 0x010** | UartOut[0:3] |
| 0x037 – 0x02C | LVDSIn[0:11] | **0x01F – 0x014** | LVDSOut[0:11] |
| 0x03F – 0x038 | XTTLIn[0:7] | **0x033 – 0x020** | XTTLOut[0:19] |

The mux and synchronizer blocks can also be described in the following data flow diagram.

A screenshot of a computer screen

Description automatically generated

## BER Block

This block contains multiple registers for signal comparison. The BER test is conducted for a finite period of time and sums up the detected bit errors between each Mux and Demux pair. The logic compares both the positive and negative edge aligned bitstreams to the test sequence at three different frequencies (150Mhz, 30Mhz, 1Mhz). When a test is completed the BER block sends its results to the BER register file.

## Control

This block rotates through all the input signals. For each input signal, it rotates through each output signal. For each input signal type, a different output bit rate is used for the PN23. Each combination of input/output is held for approximately 0.1 milliseconds.

## Signal Generator

This block takes a frequency select command from the Control block and enables the PN23 block at the desired rate/frequency. There are six frequency modes that can be active.

|  |  |
| --- | --- |
| Frequency Select | Description |
| Zero | Holds the output signal to zero. |
| High | Holds the output signal to one. |
| Pulse | Sends regular pulses that are 3x the period of TTL signals |
| LVDS | Sends a PN23 bitstream at 150Mhz |
| RS422 | Sends a PN23 bitstream at 30Mhz |
| TTL | Sends a PN23 bitstream at 1Mhz |

## BER Register File

This block keeps track of successful loopback connections and the bit error rate associated with each. The register file has two sections: the test registers, and the info registers. For the BER test all registers are addressed in the same space, meaning that the signal address from the BER block is offset by the number of info registers. For more detail on addressing look to the table under the register file sub section.

The BER results are read from the USB host interface so the frequency and content can be analyzed externally via the bertvs python script.

## Host Interface

This block connects the USB interface to the register file via the register bridge. Additionally, the reset signal can be issued from wire out endpoints.

# Operation

The intended operation of this TVS FPGA design is simple. Power on the TVS, load the bit file, then connect and disconnect each loopback plug to each front panel connector. Throughout this process, USB host software can read the contents of the register file to see the status and progress of each input and each output.

## BER Calculation

During the test there are varying rates that each signal is tested at. The rate is solely based on the clock rate for a given signal. For instance, RS422 will operate at 30 MHz and the sampling rate will be 150MHz for higher timing resolution, every time a sample does not match the original signal one bit error is added.

# Software Interface

This section describes how to access the register file.

## Register File

The table below shows the register map.

|  |  |  |  |
| --- | --- | --- | --- |
| Address | R/W | Mnemonic | Description |
| 0x000 | RO | Version | Version of FPGA design |
| 0x001 | RO | Offset | Contains BER TVS address offsets |
| 0x002 | W | Command 1 | \*Used to control the BER test externally if requested |
| 0x003 | W | Command 2 | ^^^ |
| 0x004 – 0x007 | RO | Failsafe Status | Contains the failsafe statuses for signals 31:0 |
| 0x008 – 0x029 | RO | RS422In[0:39] | RS422 BER |
| 0x030 – 0x033 | RO | UartIn[0:3] | Uart BER |
| 0x034 – 0x03F | RO | LVDSIn[0:11] | LVDS BER |
| 0x040 – 0x053 | RO | XTTLOut[0:19] | XTTL BER |

\*Not implemented

## Register Definition

### Version Register

This register reports the current bit file the FPGA has loaded. The version is reported as a 32-bit integer.

### Offset Register

The offset register contains the offsets for signal types within the TVS. These offsets are meant to be configurable in the ber\_tvs header file and read in by software to adapt to any hardware changes. Note that the offsets are relative to each other and are calculated cumulatively in this order: RS422, Uart, LVDS, TTL.

|  |  |  |  |
| --- | --- | --- | --- |
| Field | R/W | Default Value | Description |
| RS422\_Offset [5:0] | RO | 40 | The number of RS422 signals |
| Uart\_Offset [11:6] | RO | 4 | The number of Uart signals |
| LVDS\_Offset [17:12] | RO | 12 | The number of LVDS signals |
| TTL\_Offset [23:18] | RO | 20 | The number of TTL signals |
| Unused [31:23] | RO | 0 |  |

### Command Register

The command register is a field that can be written to via the Opal Kelly host interface allowing the user to control the TVS test procedure without restarting the device or loading a new bit file.

|  |  |  |  |
| --- | --- | --- | --- |
| Field | R/W | Default Value | Description |
| Command [31:0] | W | 0 | In development |

### Failsafe Status Register

The failsafe status register contains status bits for each differential signal. All signals are given a single bit value corresponding to their address within the TVS. Currently out of the 128 bits that can be assigned 56 are used, meaning that only failsafe status registers 1 and 2 are active.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Register | Field |  | R/W | Default Value | Description |
| failsafe | **RS422 [31:0]** |  | RO | 40 | The number of RS422 signals |
|  | **RS422 [11:6]** |  | RO | 4 | The number of Uart signals |
|  | **LVDS\_Offset [17:12]** |  | RO | 12 | The number of LVDS signals |
|  | **TTL\_Offset [23:18]** |  | RO | 20 | The number of TTL signals |

### BER Test Registers

The BER test registers contain the total number of bit errors per test. Within each register there are two counters and a delay associated with the signal.

|  |  |  |  |
| --- | --- | --- | --- |
| Field | R/W | Default Value | Description |
| BER [25:0] | RO | 0x00ff\_ffff | BER count |
| Delay [30:26] | RO | 0x001f | The number of clock cycles |
| Connection [31:31] | RO | 0x0000 | Connection status flag |

|  |  |  |  |
| --- | --- | --- | --- |
| Field | R/W | Default Value | Description |
| LVDS\_BER [19:0] | RO | 0xfff\_ffff | TTL BER count |
| Delay [31:20] | RO | 0xf | The number of clock cycles |

## Wire In Definition

This wire in is the only wire in definition and it allows the software API to set the reset of the HDL code and start running the tests. Only 1 bit of the 32-bit output bus is used to initially set and reset the HDL. The address map is shown in the following table

|  |  |  |  |
| --- | --- | --- | --- |
| EpAddress | R/W | Mnemonic | Description |
| 0x000 | WO | Reset | Initial reset of FPGA design |

# FPGA Target

This design supports testing of the TVS using the XEM7310 Opal Kelly daughter card. This section provides implementation details for the FPGA target.

## XEM7310

The Opal Kelly XEM7310 contains a Xilinx Spartan-7 family FPGA with model number XC7A200-1FGG484. This daughter card is found in the TVS-XEM7310-A20.

### FPGA Pin-Out

This section describes the pin-out of the FPGA for various targets.

| Signal | Dir | Type | FPGA Pin  XEM3010 | FPGA Pin  XEM6310 | FPGA Pin  XEM7310 |
| --- | --- | --- | --- | --- | --- |
| RS422 Inputs | | | |  |  |
| RS422In\_0 | In | LVCMOS33 | K15 | P21 | H3 |
| RS422In\_1 | In | LVCMOS33 | J13 | R20 | H2 |
| RS422In\_2 | In | LVCMOS33 | H13 | R22 | G2 |
| RS422In\_3 | In | LVCMOS33 | J14 | P22 | G3 |
| RS422In\_4 | In | LVCMOS33 | J18 | N22 | F1 |
| RS422In\_5 | In | LVCMOS33 | H14 | N20 | G1 |
| RS422In\_6 | In | LVCMOS33 | J15 | M21 | E2 |
| RS422In\_7 | In | LVCMOS33 | G14 | M22 | D2 |
| RS422In\_8 | In | LVCMOS33 | N15 | F17 | L4 |
| RS422In\_9 | In | LVCMOS33 | P17 | D19 | R1 |
| RS422In\_10 | In | LVCMOS33 | P16 | F16 | L5 |
| RS422In\_11 | In | LVCMOS33 | P18 | D20 | P1 |
| RS422In\_12 | In | LVCMOS33 | L18 | L15 | J6 |
| RS422In\_13 | In | LVCMOS33 | L16 | J16 | L1 |
| RS422In\_14 | In | LVCMOS33 | K13 | K20 | L3 |
| RS422In\_15 | In | LVCMOS33 | K18 | K19 | K3 |
| RS422In\_16 | In | LVCMOS33 | E18 | G22 | V15 |
| RS422In\_17 | In | LVCMOS33 | F17 | G20 | U15 |
| RS422In\_18 | In | LVCMOS33 | D18 | E22 | T15 |
| RS422In\_19 | In | LVCMOS33 | D17 | C20 | W14 |
| RS422In\_20 | In | LVCMOS33 | L15 | K16 | M1 |
| RS422In\_21 | E3In | LVCMOS33 | M16 | K17 | M5 |
| RS422In\_22 | In | LVCMOS33 | M15 | J17 | M6 |
| RS422In\_23 | In | LVCMOS33 | N17 | F18 | M3 |
| RS422In\_24 | In | LVCMOS33 | T16 | G16 | P5 |
| RS422In\_25 | In | LVCMOS33 | T17 | G17 | P4 |
| RS422In\_26 | In | LVCMOS33 | R16 | H19 | N4 |
| RS422In\_27 | In | LVCMOS33 | P15 | H18 | N3 |
| RS422In\_28 | In | LVCMOS33 | E17 | E20 | T14 |
| RS422In\_29 | In | LVCMOS33 | G15 | F21 | K4 |
| RS422In\_30 | In | LVCMOS33 | C18 | C22 | Y14 |
| RS422In\_31 | In | LVCMOS33 | B18 | A20 | Y12 |
| RS422In\_32 | In | LVCMOS33 | L17 | M16 | K6 |
| RS422In\_33 | In | LVCMOS33 | M18 | F19 | M2 |
| RS422In\_34 | In | LVCMOS33 | L13 | U22 | H5 |
| RS422In\_35 | In | LVCMOS33 | L14 | U20 | J5 |
| RS422In\_36 | In | LVCMOS33 | T18 | F20 | N5 |
| RS422In\_37 | In | LVCMOS33 | U18 | G19 | P6 |
| RS422In\_38 | In | LVCMOS33 | R18 | J19 | N2 |
| RS422In\_39 | In | LVCMOS33 | R17 | H20 | P2 |
| Uart1\_Rx | In | LVCMOS33 | F4 | A12 | AA14 |
| Uart2\_Rx | In | LVCMOS33 | C17 | B22 | V14 |
| Uart3\_Rx | In | LVCMOS33 | C16 | A21 | Y11 |
| Uart4\_Rx | In | LVCMOS33 | E3 | B14 | AA13 |
| RS422 Outputs | | | |  |  |
| RS422Out\_0 | Out | LVCMOS33 | H16 | L22 | E3 |
| RS422Out\_1 | Out | LVCMOS33 | F14 | L20 | F3 |
| RS422Out\_2 | Out | LVCMOS33 | H15 | H21 | B1 |
| RS422Out\_3 | Out | LVCMOS33 | G16 | H22 | A1 |
| RS422Out\_4 | Out | LVCMOS33 | H18 | L19 | D1 |
| RS422Out\_5 | Out | LVCMOS33 | J17 | M20 | E1 |
| RS422Out\_6 | Out | LVCMOS33 | H17 | K21 | C2 |
| RS422Out\_7 | Out | LVCMOS33 | G18 | K22 | B2 |
| RS422Out\_8 | Out | LVCMOS33 | F15 | F22 | J4 |
| RS422Out\_9 | Out | LVCMOS33 | E16 | D21 | T16 |
| RS422Out\_10 | Out | LVCMOS33 | E15 | D22 | U16 |
| RS422Out\_11 | Out | LVCMOS33 | D16 | B21 | V13 |
| RS422Out\_12 | Out | LVCMOS33 | N14 | V21 | K2 |
| RS422Out\_13 | Out | LVCMOS33 | M14 | V22 | J2 |
| RS422Out\_14 | Out | LVCMOS33 | K13 | T21 | K1 |
| RS422Out\_15 | Out | LVCMOS33 | K14 | T22 | J1 |
| Uart1\_Tx | Out | LVCMOS33 | C2 | A16 | W16 |
| Uart2\_Tx | Out | LVCMOS33 | D3 | B16 | W15 |
| Uart3\_Tx | Out | LVCMOS33 | E4 | A14 | AB13 |
| Uart4\_Tx | Out | LVCMOS33 | C3 | B18 | AA16 |
| LVDS Inputs | | | |  |  |
| RxData\_J6 | In | LVCMOS33 | G1 | A10 | U1 |
| RxStrobe\_J6 | In | LVCMOS33 | F2 | C13 | AA1 |
| RxData\_J7 | In | LVCMOS33 | E1 | A13 | AB1 |
| RxStrobe\_J7 | In | LVCMOS33 | E2 | C15 | AB16 |
| RxData\_J8 | In | LVCMOS33 | J1 | A4 | V2 |
| RxStrobe\_J8 | In | LVCMOS33 | J2 | B8 | W2 |
| RxData\_J9 | In | LVCMOS33 | H1 | A8 | Y2 |
| RxStrobe\_J9 | In | LVCMOS33 | H2 | B10 | T1 |
| RxData\_J10 | In | LVCMOS33 | K2 | D7 | AB7 |
| RxStrobe\_J10 | In | LVCMOS33 | L1 | D17 | AB5 |
| RxData\_J11 | In | LVCMOS33 | K5 | L17 | R3 |
| RxStrobe\_J11 | In | LVCMOS33 | K1 | D8 | AB6 |
| LVDS Outputs | | | |  |  |
| TxData\_J6 | Out | LVCMOS33 | D2 | C17 | AA15 |
| TxStrobe\_J6 | Out | LVCMOS33 | D1 | A15 | AB17 |
| TxData\_J7 | Out | LVCMOS33 | C1 | A17 | AB15 |
| TxStrobe\_J7 | Out | LVCMOS33 | B1 | A18 | Y16 |
| TxData\_J8 | Out | LVCMOS33 | J6 | D6 | Y3 |
| TxStrobe\_J8 | Out | LVCMOS33 | K4 | K18 | R2 |
| TxData\_J9 | Out | LVCMOS33 | J5 | C6 | AA3 |
| TxStrobe\_J9 | Out | LVCMOS33 | J4 | A3 | U2 |
| TxData\_J10 | Out | LVCMOS33 | N2 | D14 | T5 |
| TxStrobe\_J10 | Out | LVCMOS33 | P1 | A5 | V5 |
| TxData\_J11 | Out | LVCMOS33 | M1 | C14 | U5 |
| TxStrobe\_J11 | Out | LVCMOS33 | L2 | E16 | AA5 |
| xTTL Inputs | | | |  |  |
| XTTLI\_0 | Input | LVCMOS33 | T3 | T19 | V9 |
| XTTLI\_1 | Input | LVCMOS33 | T2 | T20 | V8 |
| XTTLI\_2 | Input | LVCMOS33 | R2 | U19 | R6 |
| XTTLI\_3 | Input | LVCMOS33 | T1 | W22 | Y9 |
| XTTLI\_4 | Input | LVCMOS33 | R3 | P17 | V7 |
| XTTLI\_5 | Input | LVCMOS33 | U1 | W20 | W9 |
| XTTLI\_6 | Input | LVCMOS33 | P2 | C5 | U6 |
| XTTLI\_7 | Input | LVCMOS33 | R1 | V20 | T6 |
| xTTL Outputs | | | |  |  |
| XTTLO\_0 | Out | LVCMOS33 | G4 | B12 | Y13 |
| XTTLO\_1 | Out | LVCMOS33 | G3 | A9 | AB2 |
| XTTLO\_2 | Out | LVCMOS33 | H3 | A7 | Y1 |
| XTTLO\_3 | Out | LVCMOS33 | H4 | C9 | AB3 |
| XTTLO\_4 | Out | LVCMOS33 | F5 | C7 | W1 |
| XTTLO\_5 | Out | LVCMOS33 | G5 | A6 | V3 |
| XTTLO\_6 | Out | LVCMOS33 | H6 | C16 | AB8 |
| XTTLO\_7 | Out | LVCMOS33 | H5 | B6 | U3 |
| XTTLO\_8 | Out | LVCMOS33 | K6 | D15 | AA8 |
| XTTLO\_9 | Out | LVCMOS33 | L6 | C12 | AA6 |
| XTTLO\_10 | Out | LVCMOS33 | M5 | C10 | AA4 |
| XTTLO\_11 | Out | LVCMOS33 | L5 | D11 | Y6 |
| XTTLO\_12 | Out | LVCMOS33 | N5 | D10 | Y4 |
| XTTLO\_13 | Out | LVCMOS33 | L3 | C8 | T4 |
| XTTLO\_14 | Out | LVCMOS33 | M3 | R19 | W5 |
| XTTLO\_15 | Out | LVCMOS33 | L4 | D9 | R4 |
| XTTLO\_16 | Out | LVCMOS33 | M4 | P18 | W6 |
| XTTLO\_17 | Out | LVCMOS33 | N4 | M18 | Y7 |
| XTTLO\_18 | Out | LVCMOS33 | P4 | N16 | W7 |
| XTTLO\_19 | Out | LVCMOS33 | P3 | M17 | Y8 |